Metal-Coated SU-8 Structures for High-Density 3-D Microelectrode Arrays

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***Abstract*— Electric fields can be effectively used to sense, manipulate, and move particles in lab-on-a-chip devices. Nevertheless, the throughput of such devices is a critical issue, which can be effectively improved by increasing the height of the microchannels. For this purpose, vertical electrodes are needed in order to apply electrical stimuli homogeneously over the full height of the channel. In this paper, we propose different fabrication processes based on a conformal coating of 3-D SU-8 structures with metal layers, defining vertical electrodes in microfluidic channels with high aspect ratio and uniform coating of the vertical sidewalls. We describe two different strategies to achieve the patterning of connection lines inside the gaps of the pillar electrodes—one based on liftoff and the other based on dry film resist. We show how the liftoff approach allows for high connection densities and high resolution of the patterning inside the 3-D electrode arrays. Moreover, we highlight how the dry film process provides an efficient and low-cost alternative when neither high-density patterning nor high resolution is needed. Standard resistive and impedance measurements show high conductivity of the structures whose fabrication process grants standard photolithographic resolution in the definition of the electrode features. [2016-0002]**

***Index Terms*— 3D microelectrodes, microelectrode arrays, SU-8, SU-8/PDMS bonding, vertical electrodes.**

I. Introduction

ELECTRIC-FIELD based techniques for microparticle sensing and manipulation in microsystems have been employed for numerous purposes. Their applications encompass sensing and analyzing bio-particles by impedance spectroscopy [1] or electrorotation [2]; moving, positioning, and trapping particles by dielectrophoresis [3]; manipulating cells to attain electrofusion [4], electroporation [5] or cell lysis [6]. A common feature of these devices is represented by planar electrodes that apply the electric potentials only from the bottom of the channels, resulting in an electric field that quickly decreases with increasing channel heights. Technological solutions allowing to apply electrical signals homogenously across the full channel height are hence required. Along this line, vertical electrodes represent an ideal solution to increase the efficiency of lab-on-a-chip applications, especially when working with high microfluidic channels.

Several processes have been proposed to fabricate vertical or 3D microelectrodes, namely standard [3], [7], [8] and electrodeless [9], [10] electroplating, pyrolysis of polymeric precursors to achieve carbon structures (C-MEMS) [11] a combination of electroplating, sputtering and laser scribing [12] and the use of metal ion implantation [13]. Electroplating can be difficult to control and requires a long and expensive process that might result in low-quality surfaces. Furthermore, the fabrication of structures with high-aspect ratio gaps through electroplating is difficult to achieve [14]. Electrodeless electroplating is based on the use of a femtosecond laser and the writing is done in a serial way, leading to long processing times. Furthermore, this process results in a high surface roughness [10]. The C-MEMS process is a rapid way to create 3D structures; nonetheless, the conductivity of carbon is four orders of magnitude lower than the one of metals. Moreover, pyrolysis leads to the shrinkage of the precursors [15], which in turn causes important design constraints. The combination of electroplating with sputtering and laser scribing, apart from being an overall more complex process, suffers from the above mentioned issues [12]. Regarding metal ion implantation, as the process is based on the use of a shadow mask only limited resolution and density of structures can be achieved. Furthermore, one metal ion implantation step is only effective for a certain orientation of the sidewalls and thus several steps are needed to obtain facing electrodes or fully-coated 3D structures [13].

We propose a solution to achieve vertical high conductive electrodes based on SU-8 photolithography, standard thin-film deposition and patterning techniques, which enables the simultaneous integration of 3D microelectrodes and microchannels. We chose to use SU-8 as it is an inexpensive material to fabricate structures with high-aspect [16] and gap ratios [17] and because it offers good chemical resistance [16]–[18]. In addition, SU-8 enables high resolution patterning [17], [18] and it results in structures with straight and smooth sidewalls [16], [17]. Despite these advantages, SU-8 requires additional processing to obtain functional electrodes due to its insulating properties. Mixing silver nanoparticles into the SU-8 [19] or turning it into carbon structures by the above mentioned C-MEMS process [11] were suggested in the past; nevertheless, both approaches lead to a conductivity much lower than the one of metal.

In a previous publication [20], we described 3D electrodes based on homogenous metal coating of silicon connected by

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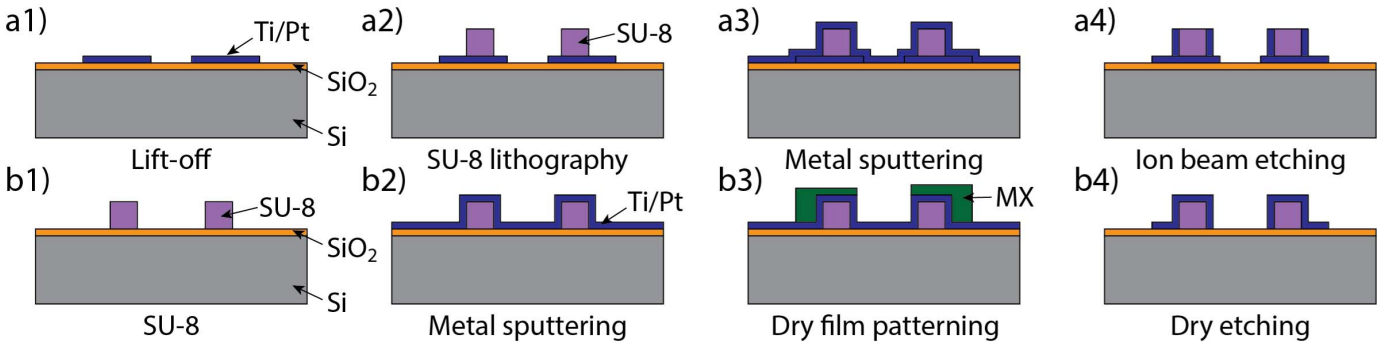

Fig. 1. Schematic of the two proposed fabrication processes for free-standing pillar electrodes. The patterning of connection lines by means of lift-off (a1-a4) and dry film resist (b1-b4) are illustrated. Planar connection lines are patterned by lift-off (a1) and SU-8 pillars are patterned on top of the wires (a2). The electrodes are covered with a metal film by metal sputtering (a3) and the metal on horizontal surfaces is etched away by means of dry etching (a4). Alternatively, the SU-8 pillars are patterned (b1) and covered with a metal layer by sputter deposition (b2). A dry film resist is then applied (b3) that serves as etch mask for dry etching (b4).

planar wires realized by means of spray coating and metal etching. On the other hand, in this paper, we propose the use of SU-8 (instead of silicon) to reduce time and cost of fabrication and to eliminate electrical parasitics coming from the substrate and the pillar core. In order to accomplish the adhesion of the metal layer to the SU-8 micropillars, we define the most suitable formulation by investigating the role of different SU-8 post-processing steps. The development of the SU-8 structures is shown both on silicon and glass substrates. We present a strategy to achieve high connection-density making use of the additive nature of the SU-8 fabrication process. This involves, at first, the patterning of the connection lines and, successively, the definition of the 3D SU-8 topography. In addition, we propose an alternative fabrication process based on the patterning of the electrode connections by dry film photoresist. The main advantages of this process are reduced cost and simplicity, although, due to the lower resolution of the film resist, it is limited to cases with large critical dimensions of the connection lines.

Finally, we integrate the vertical electrodes into microfluidic channels and show that it is possible to achieve electrodes that span the full height of the channel, without further process optimization. Our design provides microfluidic accesses through the back of the chips and sealing of the channels promoted by PDMS-mediated bonding of a microscope glass coverslip by a vapor-phase silanization method [21]. This enables the use of bulky lenses with short working distances while keeping at the same time the chip footprint minimal.

II. Materials and Methods

A. Fabrication of Metal-Coated SU-8 Structures

A 50 μm-thick SU-8 (Gersteltec GM 1070) layer is applied by spin coating at 1600 rpm, with a soft-bake performed at 90 °C for 5 min and a UV exposure at a dose of 400 mJ/cm^2 (Karl Süss MJB 4). A post-exposure bake at 90 °C for 30 min is then performed to catalyze cross-linking, followed by development in propylene-glycol-monomethyl-ether-acetate (PGMEA). Finally, the SU-8 is hard-baked at 135 °C for 2 h, in order to improve the adhesion of the metal layer (Fig. 1 a2 and b1). The SU-8 surface is then activated by oxygen plasma (Tepla 300, 400 ml/min O_2, 500 W, 30 s) and metallized. Metallization is performed by sputter coating (Alliance Concept DP 650) resulting in the ions hitting the target with a random incident angle upon colliding with the sputtering gas. The sputtering is performed with a distance of 80 mm between the target and the wafer, without rotation of the latter. Argon plasma pressure is $5 \cdot 10^{-3}$ mbar and DC power is 400 W for Ti and 250 W for Pt. 20 nm of Ti are deposited at an average rate of 3.1 Ås^{-1} and 200 nm of Pt at 6.7 Ås^{-1} (Fig. 1 a3 and b2).

B. Patterning of Connection Lines

1) Patterning of Connection Lines Achieving High Precision and High Density: In order to achieve a higher density of connection lines, these are patterned by lift-off on the plain substrate prior to the fabrication of the SU-8 structures. To this aim, a double layer of lift-off and AZ1515 resist is applied by spin coating (EVG 150 automatic coater), exposed with a dose of 24 mJ/cm^2 (Karl Süss MA/BA 6) and developed by spray development (EVG 150 automatic coater). A triple metal layer (20 nm Ti, 200 nm Pt and 20 nm Ti) is evaporated by e-beam (Leybold Optics Lab 600H) followed by dissolution of the underlying photoresist in a remover bath (Remover 1165) (Fig. 1 a1). The 3D electrodes are then obtained by patterning the SU-8 on top of the connection lines and by sputtering metal layers, as described in section II.A (Fig. 1 a2 and a3). Anisotropic ion beam etching with argon ions (Veeco Nexus IBE 350) is then performed on the full wafer without any mask. This allows removing the second horizontal metal layer while preserving the vertical metal features. The etching process is monitored by a secondary ion mass spectrometer (SIMS) to limit the etching into the planar layer previously deposited for the connections (Fig. 1 a4).

2) Low-Cost Technique for the Patterning of Connection Lines: The connection lines are patterned by means of a dry film resist (DuPont MX 5050) laminated at 95 °C, subsequently exposed with a 105 mJ/cm^2 dose (Karl Süss MJB 4) and developed in MRD 4000/75 IC (Microresist Technology GmbH) (Fig. 1 b3). The patterned dry film resist serves as a mask during the dry etching process of the metal film

(Veeco Nexus IBE 350). The resist is finally stripped away in sodium hydroxide (NaOH 2.5M) (Fig. 1 b4).

C. Integration of 3D Pillars Into Microfluidic Channels

1) Fabrication of Microfluidic Structures: SU-8 microfluidic structures are processed on the wafer after the fabrication of the 3D electrodes by the same SU-8 fabrication process used for the pillar cores, with the exclusion of the hard-baking step (Section II.A).

2) Fabrication of the Microfluidic Accesses Through the Substrate: A process based on the use of a shadow mask is employed to chips. The mask is fabricated starting from a silicon wafer presenting a top 2 μm SiO_2 layer. A 4 μm-thick photoresist (AZ ECI 3007) is then applied by means of an automatic coating system (Rite Track 88 series) and exposed on a mask aligner (Karl Süss, MA/BA 6, 190 mJ/cm^2). The pattern is transferred into the SiO_2 layer and 400 μm-deep into the silicon wafer by dry etching (Alcatel 601E). Both the photoresist and the SiO_2 layer are then stripped (Remover 1165 and BHF) and the wafer is subsequently ground from the back to complete the opening of the etch holes (Disco DAG 810). Finally, a 4 μm Al protection layer is sputtered to protect the top of the shadow mask (Pfeiffer Spider 600).

The shadow mask is then fixed to the wafer, which features the 3D electrodes and microfluidic trenches, (Subsections II A-B). Its adhesion is guaranteed by means of a special wax (Quick Stick 135), which is deposited on the mask before alignment (Idonus, shadow mask aligner). The stack, composed of the shadow mask and the wafer, is then heated above 100 °C in order to melt the wax and provide sticking. The front SiO_2 layer of the wafer is subsequently etched (Alcatel 601E) and the pattern is transferred 400 μm deep into the silicon by means of Bosch etching (Alcatel 601E). Finally, the backside of the wafer is ground (DAG 810) to open up the microfluidic access holes and to separate the single chips.

3) Microfluidic Sealing: The chips are sealed by microscope glass coverslips that present a thin and uniform PDMS layer on one side. The preparation of the coverslip is carried out as described hereafter. We use a dummy wafer as a substrate on which we laminate a thick-film resist (DuPont MX 5050, 95 °C). The protection foil that comes with the thick-film resist is not removed as it is employed later to separate the PDMS-coated glass slides from the substrate. A PDMS layer (mix ratio 10:1, 2000 rpm, SCS 6800) is spin-coated onto the wafer, and the microscope coverslip is then placed on it. The PDMS is degassed in a vacuum chamber and baked for 2 h at 80 °C to catalyze crosslinking. Finally, coverslip and PDMS are stripped from the dummy wafer by means of the protective foil. The PDMS is finally cut to match the size of the glass coverslips. The protective foil is removed only prior to bonding of the PDMS-coated coverslip to the chip. This step is performed by oxygen plasma activation (Diener electronic Femto, 100 W, 0.6 Pa, 1 min) and silanization of the PDMS-coated cover slip. The latter is performed by placing a flask with (3-Aminopropyl)triethoxysilan (APTES) in a vacuum desiccator. After building up the vacuum, we close the chamber and leave the flask together with the coverslip for 2 h) in order to catalyze polymerization.

D. Electrical Characterization of the 3D Electrodes

Electrical characterization of the 3D electrodes was performed both in air and in the presence of electrolyte solutions. The tests allowed to verify the conductivity of the 3D electrodes, their connection to the planar metal lines and the proper exposure of the electrode surface. The test structures were realized with the process described in Subsection II B.2, which grants high resolution of the planar lines. We developed test structures to assess the resistive contribution of the pillars, which consisted of planar lines interrupted by 20 μm gaps shorted by 3D pillars (Fig. 5a). The electrical resistance was extracted by applying a voltage sweep from -5 V to 5 V (Agilent 4155C Semiconductor Parameter Analyzer, Süss PM8 manual probe station). Moreover, vertical electrodes with lengths varying from 200 μm to 800 μm were measured (Keithley 2400) to extract the sheet resistance of the vertical metal layers (sidewalls). To verify the exposure of the 3D electrode-sidewalls, the microfluidic structures were filled with an electrolyte solution (PBS 1X), leading to the generation of a double layer capacitance at the electrodes/solution interfaces. This parameter has been characterized by impedance spectroscopy (Zürich Instruments, HF2TA transimpedance amplifier and HF2LI Lock-in amplifier) to assess the presence of the double layer capacitance and to observe its dependence on the exposed area of the pillar. Test structures are represented in Fig. 6a. Pillars were embedded into the channels sidewalls, extruding of a distance d' of 15 μm and their length L ranged from 30 to 500 μm. Two types of electrodes were characterized with either 100 or 200 μm inter-electrode spacing.

III. Results

A. Adhesion of Metal Layers on SU-8 Structures

The adhesion of the metal to the SU-8 pillars is a critical feature of the process. We found that adhesion was more critical for bigger structures than for small ones, especially without hard-baking of the SU-8. On our test structures adhesion was improved by both hard-baking and oxygen plasma activation prior to metal deposition. Furthermore, we observed that a short oxygen plasma treatment (500 W, 30 s) was a good compromise between achieving good adhesion and avoiding significant etching of the hard-baked SU-8 pillars.

B. Patterning of the Connection Lines

1) Patterning of Connection Lines by Lift-Off: Lift-off processing was used to define connection lines prior to SU-8 fabrication and metal sputtering. In this case the most critical step is the mask-less ion-beam etching. In order to prevent excessive thinning of the previously patterned lines, SIMS was used to monitor the etching process and stop it before critically etching into the first metal layer. We developed a variety of 3D pillars with a height of 50 μm and spacing, down to 10 μm. In addition, the process allows high patterning resolution of

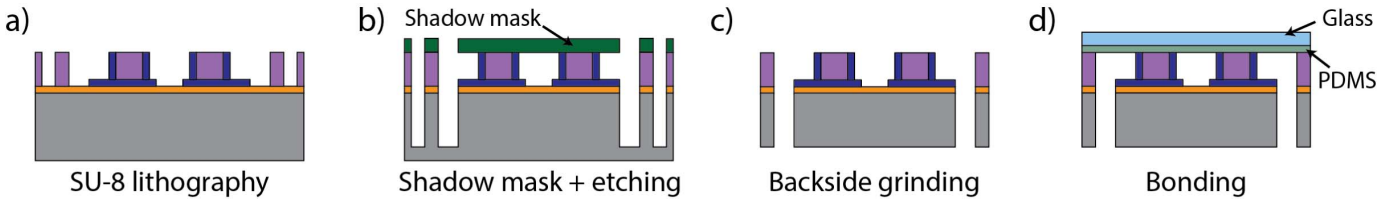

Fig. 2. Schematic of the integration of 3D electrodes into microfluidic channels. Microfluidic structures are defined by an SU-8 lithography step (a) and backside microfluidic accesses, as well as chip outlines, are etched into the substrate by dry etching with a shadow mask (b). The wafer is then ground from the backside to open microfluidic connections and to separate the single chips (c). Finally, the microfluidic channels are sealed by bonding a thin PDMS-coated glass slide on top of the microfluidic channel (d).

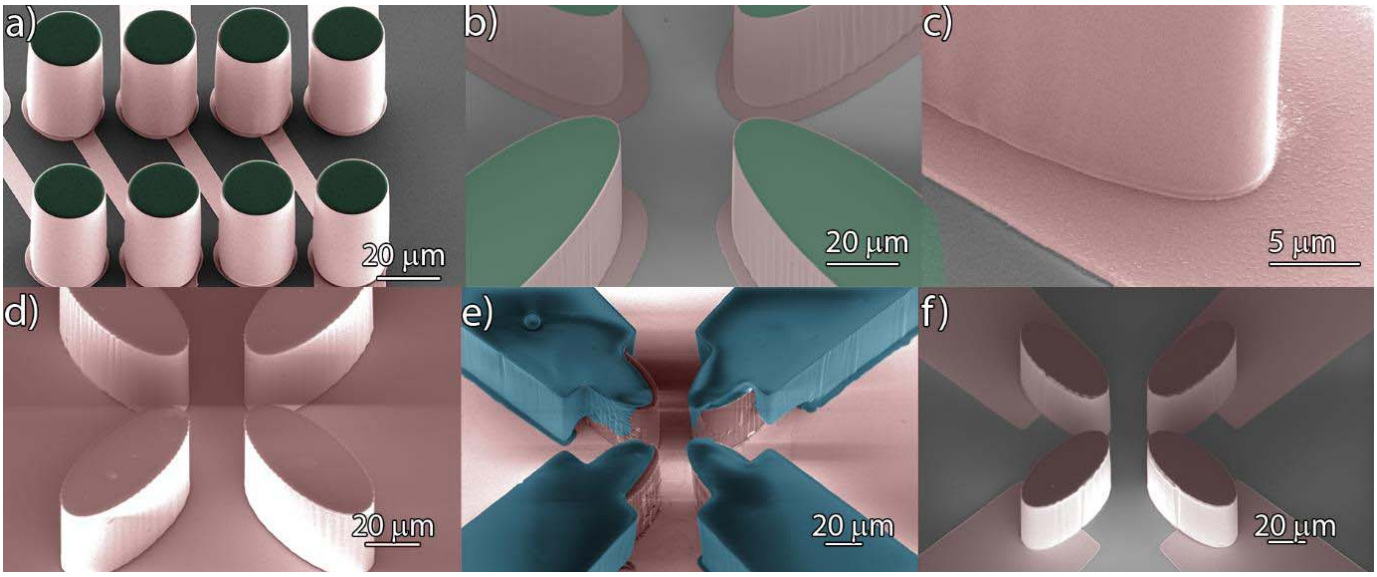

Fig. 3. SEM imaging of metal-coated 3D SU-8 pillars (all structures are 50 μm high). Structures resulting from a process making use of lift-off for planar line patterning prior to SU-8 fabrication (a-c). Planar and vertical features combined to show the alignment outcome (b); close up suggesting conformity of the metal layer (c). Dry film based approach to pattern the planar lines (d-f). SU-8 structures homogenously coated with metal (d); post-processing of dry film resist to define the connection lines on the back of the pillars (e); structures resulting after metal etching and dry film stripping (f).

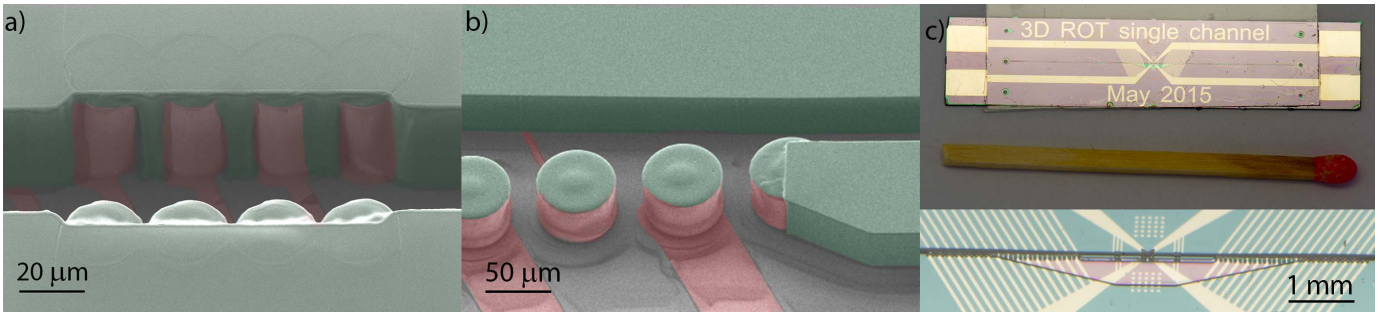

Fig. 4. SU-8 microfluidic channels integrating 3D electrodes. SEM imaging of sidewall-integrated and free-standing electrodes spanning the entire height of the channel (a-b); picture of the chip with PDMS-coated coverslip to seal the channel and a close up image of the central part of the channel, showing the 3D electrodes inside the microfluidic channel (c).

the connection lines; in this work, we designed lines down to 5 μm in width (Fig. 3a). The 3D features are then aligned with photolithographic precision to the planar wires, granting high flexibility when designing the electrodes combing planar and vertical features (Fig. 3b). Critical aspects for this approach are the connection between planar and vertical metal structures, as well as the homogenous metal coverage of the vertical sidewalls. Besides the electrical measurements reported in Section III.D, we performed SEM imaging (Fig. 3) and EDX spectroscopy (data not shown) to confirm the presence of the metal layer on the sidewalls.

2) Dry Film Resist Patterning: The outcome of the process depending on dry film resist is shown in Fig. 3 d-f. Dry film was applied on the metal-coated SU-8 structures to pattern the planar connection lines. Proper adhesion on the 3D metal topography could only be achieved by 50 μm-thick films in combination with a dry film pattern designed to overlap the pillars and exceed on the sidewalls (Fig. 3e). The outcome

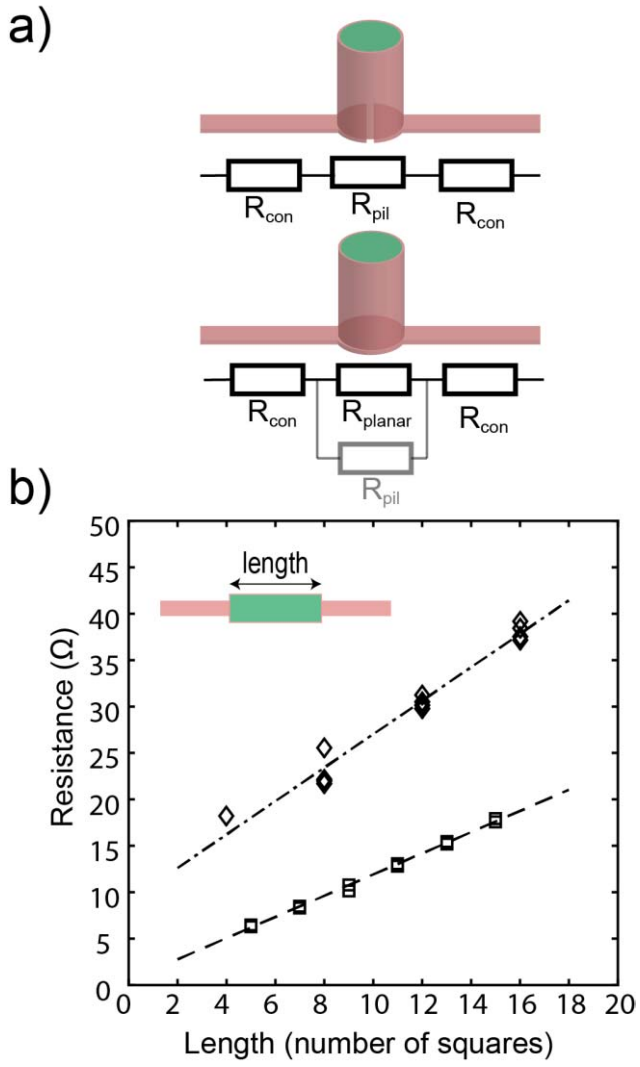

Fig. 5. (a) Cartoon of the test structures employed to quantify the resistivity of the 3D pillar (red: platinum, green: SU-8); (b) Representation of the sheet resistance of planar wires (experimental points: squares; linear fit: dashed line) and of single vertical sidewalls (experimental points: diamonds; linear fit: dashed and dotted line). Each diamond symbol corresponds to a single structure. The plot reports in total 15 measurements on 15 different structures (diamonds) plus measurements performed on the planar wires (squares). The inset is a top view representation of the 3D structures.

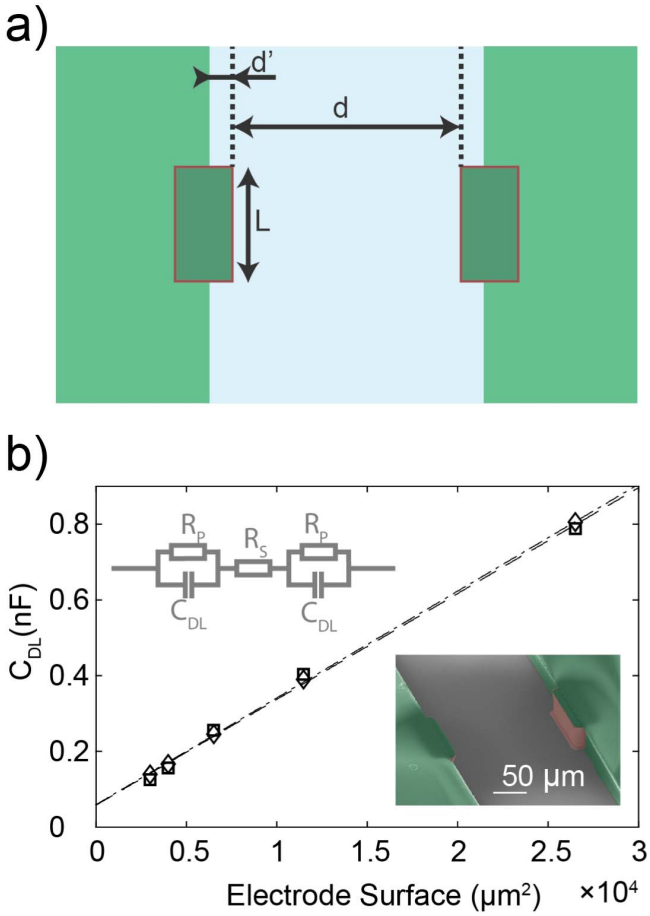

Fig. 6. (a) Cartoon representing the test structures to verify the exposure of vertical sidewalls to the solution (top view). SU-8 is indicated in green and coating metal layers in red. 3D pillars extrude by d'=15 μm from the channel main walls; (b) double layer capacitance of the single electrodes extracted by fitting the electrical equivalent model represented in the inset to a frequency spectrum acquired between 1 kHz and 10 MHz (d = 100 μm: diamonds; d = 200 μm: squares).

of the process is shown in Fig. 3f. The metalized pillars are connected to bottom lines that are patterned by dry film resist lithography.

C. Integration of the 3D Electrodes Into Microchannels

We fabricated the microfluidic structures in a second SU-8 lithography step, after the fabrication of the metal-coated 3D pillars. This enabled the alignment of channels and 3D structures with photolithographic precision. The application of the same process parameters for the two SU-8 steps resulted in microfluidic structures with a height equal to the one of the 3D pillar electrodes (Fig. 4a and 4b). In order to facilitate optical imaging on the channels, we sealed them with a standard cover slip coated with a thin PDMS layer on the side adhering to the SU-8 structures (Fig. 2d). Fig. 4c shows one chip with multiple backside accesses and four electrical connections to address 3D electrodes in the microchannels.

D. Electrical Characterization of Vertical Electrodes

The quality of the electrical connection between 3D electrodes and planar wires and the conductivity of the vertical sidewalls depends on the conformity of the metal layer deposited on the SU-8 cores. This was inspected by SEM imaging on a sample of structures and thoroughly assessed by electrical characterization. A proper connection between vertical layers and planar tracks was verified in 93% of the cases (192 3D electrodes fabricated on different wafers). In order to quantify the resistance of the connection between pillars and planar wires, the test structures depicted in Fig. 5a were fabricated. These featured up to 6 pillars in series. We evaluated the resistance of the single pillar to be $12.56 \pm 0.52\ \Omega$ by characterizing 96 different structures electrically. Besides the planar-to-vertical connection, the quality of the 3D electrodes is determined by the conductivity of vertical metal layers, which needs to ensure negligible potential drops along the electrodes height. In order to measure the sidewalls sheet resistance, we fabricated rectangular pillars of different lengths, connected by planar wires at their extremity

(Fig. 5b, inset). We first determined the sheet resistance of simple planar wires (Fig. 5b, 1.14 Ω/□, square symbols) and used it to extract the sheet resistance of vertical sidewalls, (Fig. 5b, 1.80 Ω/□ for the single sidewall, diamond symbols). Finally, we tested the exposure of vertical metal electrodes on three different microfluidic chips with 50 μm-high electrodes and channels. We injected an electrolyte solution (PBS 1X) into the microfluidic channel (Fig. 6a) and characterized the impedance of the electrode interfaces in the frequency range from 1 kHz to 10 MHz. 10 couples of identical facing electrodes with length L ranging from 30 μm to 500 μm were integrated in the channel sidewalls (Fig. 6a and Fig. 6b inset). The distance between the electrodes (d) was 100 μm or 200 μm. The electrical double layer capacitance was extracted according to the electrical equivalent model of the two electrodes represented in Fig. 6b. An average low-frequency capacitance value of 2.7 ± 0.54 μF/cm^2 was calculated, which indicates the presence of an electrochemical capacitor. The low standard deviation of the extracted interface capacitance suggests a homogeneous exposure.

IV. Discussion

In this paper we introduce a new fabrication process based on the combination of SU-8 photolithography and metal sputtering to fabricate metal-coated vertical electrodes in microfluidic channels. The density of the structures depends on the resolution of the 3D structures and on the one of the photolithography employed to pattern the planar connections by lift-off. The aspect ratio of the pillar structures depends on the SU-8 process, which can achieve aspect ratios of 20:1 and heights beyond 200 μm. The uniform metal coverage of vertical surfaces is granted by the isotropy of the sputtering, as reported in [20]. The electrical characterization performed in this work further indicates similar metal coverage on the vertical sidewalls compared to the horizontal metal wires (Fig. 6). The approach described is therefore suitable for high-density arrays of 3D electrode structures and/or high channels.

In this work, we also propose an alternative solution for the patterning of the connection lines, based on the use of dry film lithography and isotropic metal etching following the 3D pillars fabrication and metal sputtering. We show that a film thickness in the same range as the height of the 3D structures is required, which in turn limits the resolution of the planar metal lines. Moreover, to achieve sufficient adhesion, the dry film pattern defining the connection lines needs to extend out of the pillars sidewalls limiting the density of the connection lines even further. Nevertheless, this inexpensive and straightforward approach is a viable solution when the design implies large electrode spacing. Table 1 provides a comparison of two processes with respect to their limitations and the process characteristics.

The electrical characterization performed on structures built on silicon and glass proves that the vertical electrodes are connected to the planar lines through low-resistive horizontal-to-vertical paths and that the resistivity of the vertical metal layers shows only a slight increase with respect to the one of planar lines. Impedance spectroscopy on electrode pairs of different sizes and inter-electrode spacing allows us to conclude that vertical metal layers are entirely exposed.

TABLE I
Comparison of the Two Fabrication Processes

	Lift-off	Dry-film
Patterning resolution	1 μm	50 μm
Process steps	4	4
Metalization steps	2	1
Alignments	2	2
Cost	$$	$
Aspect ratio	20:1	20:1
Minimal gap[1]	40 μm	10 μm

[1]Achieved in between two 50 μm high electrode structures

The low-resistivity of the electrodes and their connections enables the use of this technology for a wide range of electrical-based lab-on-a-chip applications. In this paper we chose to fabricate platinum electrodes, nevertheless the process can be performed with any metal that can be sputtered. Some applications might require to avoid the exposure of the planar wires. In this case, it is possible to passivate the horizontal surface by evaporation of insulating layers, as illustrated in [20].

A second SU-8 process allowed to combine the 3D electrodes with microfluidic structures, either free-standing or integrated into the channel sidewalls. We showed that the height of the channel results identical to the height of the 3D electrodes by simply employing the same SU-8 processing parameters. This bears the advantage to avoid the fine-tuning of the microfluidic fabrication parameters to match the height of previous 3D structures. We achieved efficient sealing of the fluidic channels with thin coverslips by PDMS-mediated bonding. Moreover, the microfluidic accesses were realized through the chip substrate and connected on the chip backside. Thanks to this approach, the front-side is cleared from connectors facilitating the imaging of the chip.

The fabrication of the singularly addressed 3D electrodes presented in this paper and their integration in microfluidic channels was proved to work on both glass and silicon substrates, but other substrates might be possibly employed. Furthermore, the process is fully CMOS compatible, and thus opens up the possibility to integrate 3D electrodes and microfluidic channels on top of the electronic chips.

V. Conclusion

We developed a process based on SU-8 photolithography and standard thin-film deposition and patterning techniques, which enables the fabrication of 3D microelectrodes integrated in microchannels. SU-8 allows achieving high aspect-ratio and high resolution 3D electrode structures. These structures were coated with metal layers, to realize vertical electrodes with low-resistivity connections to planar wires. This technology allows creating 3D electrodes either free-standing or integrated in the channel sidewall. Our work addresses different issues, including the adhesion of the metal layers to the SU-8 and individual connections of single pillars in high-density arrays. The latter is enabled by patterning the connection lines in

a lift-off process prior to the fabrication of the 3D structures, avoiding metal patterning inside of the high topography of the 3D electrode arrays, which would limit the density of the connections and the minimum inter-electrode distance. We presented a solution to efficiently bond SU-8 to thin coverslips for channel sealing. In order to avoid patterning and critical alignment of the coverslip to the microfluidics, in- and outlets are located on the backside of the chip.

Vertical electrodes allow achieving uniform field strengths over the full channel height and lead to negligible electrical field gradient in the direction normal to the chip surface. Such features, combined with the possibility to singularly address the vertical electrodes, offer significant advantages and new design possibilities in the field of electric-based techniques for lab-on-a-chip devices. Moreover, the use of higher channels and densely packed arrays of pillars holds the promise to scale up the throughput.

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