Quasi-dry Release for Micro Electro-Mechanical Systems

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Abstract

A quasi-dry MEMS release process and release apparatus for research facilities and small volume fabrication companies is presented. The new apparatus is dedicated to the development of specialized MEMS devices that are not realizable by conventional processes.

1 Introduction

During the past decade MEMS established as commercial products. Some devices reached production volumes of several million chips a year. As an example pressure sensors and accelerometers found their way into automotive and other products and Texas Instrument's DMD became the preferred chip for image projection. Besides these "killer applications" many other MEMS proved their functionality and reliability in niche markets. The low fabrication volume of these markets is an ideal platform for start-up companies that are not able to serve a big production volume at low price per chip.

Niche markets require very specialized devices. The functionality of a MEMS is often limited by the design rules, which itself is limited by the technology that is used for the fabrication. The most critical step is the release of the movable parts by underetching the buried SiO_2 layer. Traditionally, the wafer is immersed into a bath containing liquid HF acid. The length of the undercut is controlled by the etching time.

A big inconvenience of this method is the well known sticking effect. Due to the cohesion forces of the liquid and the presence of the small gaps between the structures the released parts tend to stick permanently to other structures or the substrate. Very fragile parts can break if they come in contact with a liquid. Several methods to prevent sticking have been reported that aim to reduce surface tension or to avoid the transition from liquid to gaseous state of aggregation but they all require several additional process steps.

The use of a hydro-fluoric acid (HF) vapour phase etching (VPE) system enables the removal of silicon dioxide in a vaporous environment rather than in an aqueous solution [1]-[4]. The silicon oxide is etched in a quasi-dry method and is never in contact with a liquid. No cleaning or rinsing of the chips is needed.

IMT and *Idonus* developed and commercialized a HF VPE apparatus for research laboratories and small volume fabrication companies. The idea of the project was to

offer a powerful technology to a variety of costumers thereby helping them to launch new products that are not realizable by conventional processes.

2 HF Vapour Phase Etching

First experiments on vapour phase etching were carried out by Holmes & Snell in 1966 [5]. They observed that silicon dioxide on a wafer is etched with a comparable etch rate even when the wafer is not in the etch bath but close to. Helms & Deal [3] established that the role of the water is to provide a condensed solvent medium for the HF on the surface. Offenberg et al. [2] proposed a two step reaction where first the oxide surface is opened by formation of silanol groups by adsorbed water. Subsequently silanol groups are attacked by the HF:

$$SiO_2 + 2H_2O \rightarrow Si(OH)_4$$

$$Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O$$

The above formula shows that water acts as initiator of the etching process as well as reactant. This fact suggests that the etching process can be temperature controlled to maintain in equilibrium the amount of water needed to initiate the process and the amount of reactant water. In our vapour phase etcher this equilibrium is achieved by heating the wafer. The water film on the wafer is evaporated at moderate temperatures. The etch rate decreases with increasing temperature and stops completely at temperatures above 50℃.

The mechanical realisation of our HF VPE apparatus is shown in figure 1. It consists of a reaction chamber and a wafer holder. A heating element is integrated in the wafer holder. It controls the temperature of the wafer to be etched. Wafer clamping can be achieved in two ways: Wafers can be clamped mechanically using a clamping ring. The screwing is done from the backside of the apparatus, which is never in direct contact with the HF vapor. An electrostatic clamping mechanism allows the clamping of chips as well as wafers without the stress concentration of mechanical clamping. The backside of the wafer is protected from etching.

Liquid HF is filled into the reaction chamber. The reaction chamber is closed with the wafer holder. HF evaporates at room temperature and the etching process starts spontaneously. The etch rate is controlled by the wafer temperature that can be adjusted from 35℃ to 60℃.

After processing, the acid can be stored in a reservoir for reuse in a sealable container. Liquid transfer is simply done by lowering the communicating reservoir with a handle. Due to gravity, the acid flows into the reservoir and can be closed by two valves. Refilling the acid is done by opening the valves and lifting the handle. The acid flows into the reaction chamber. The acid can be reused for multiple etchings.

Sticking free MEMS release is achieved at etch rates up to 30 µm/h.

Figure 1: HF vapour phase etching system fabricated by *Idonus*. The design of the system was optimized for research laboratories and small volume fabrication companies. An electrostatic clamping system allows the etching of whole wafers as well as single chips.

3 Applications of the HF Vapour Phase Etching

This chapter describes the different applications HF VPE can be used for. Compared to the classical release in liquid HF very fine features can be produced with a higher yield.

3.1 Release of Silicon-On-Insulator (SOI) structures

A typical process for MEMS fabricated on SOI substrates is shown in figure 2. The fabrication starts with a bare SOI wafer consisting of a sandwich structure of a thick silicon handle wafer, a thin silicon dioxide layer and a thin silicon device layer. The device layer is patterned using a photoresist mask and Deep Reactive Ion Etching (DRIE). The etching stops at the buried oxide layer which results in very well defined microstructures. The thin silicon structures are liberated from the handle layer by selectively underetching the oxide. The latter can be done with HF but the surface tension of the acid and the following rinsing with DI water causes permanent sticking between the released structures to fixed structures on the wafer. A release with HF vapour enables sticking free release of very fragile structures with a very high yield. A DI water rinsing step is not necessary.

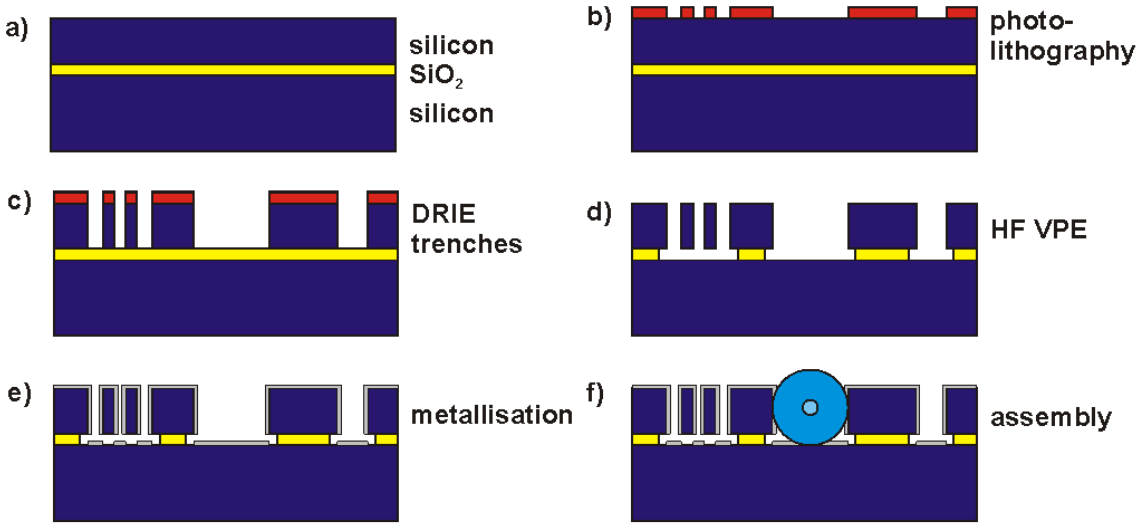

Figure 2: Fabrication process of a typical MEMS device fabricated on a SOI substrate.

As an example a microfabricated optical cross connect released with HF vapour is shown in figure 3. The process time depends on the largest silicon structure that has to be underetched by the HF. In this case, structures of 10 µm were released without sticking. The processing time was 60 minutes.

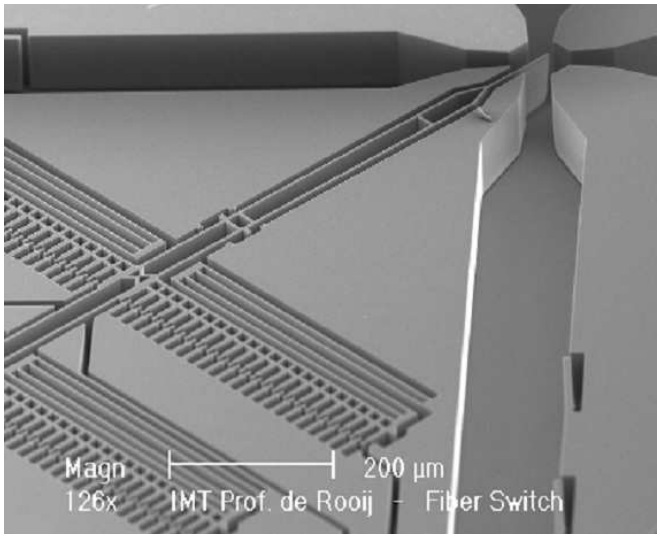

Figure 3: Microfabricated optical cross connect released with HF vapour. The oxide layer undercut measures 10 µm, the process time was 60 minutes.

3.2 Release of thin film structures

MEMS structures can be fabricated from thin films that are deposited on a thick handle wafer. Commonly used thin films are poly-silicon, silicon nitride and different

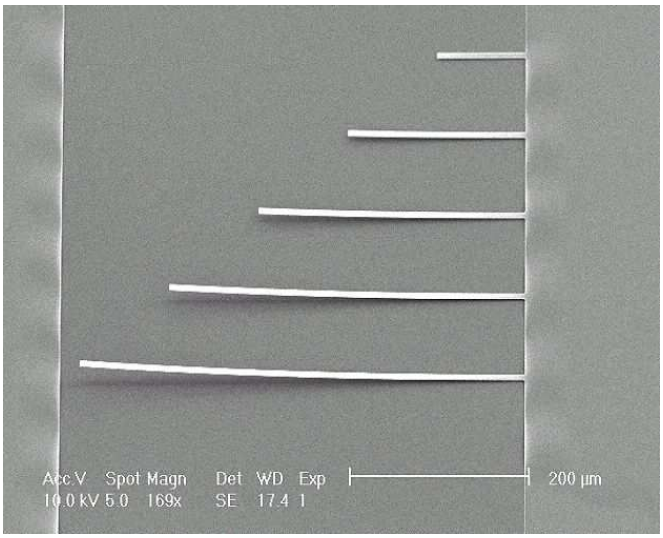

Figure 4: 0.4 µm thick poly-silicon beams released from 1 µm thermal SiO_2: The width of the beams is 10 µm, the length varies from 100 to 500 µm.

metals like aluminium or gold. These materials are deposited on sacrificial layers as polymers, silicon dioxide or metals. In order to obtain movable structures the sacrificial materials are removed selectively to the functional layers. The small thicknesses of the deposited materials require special care during the release process to prevent sticking. If silicon oxide is used as a sacrificial layer the release can be made with HF vapour. Compatible functional materials are poly-silicon, aluminium and most noble metals. Figure 4 shows 0.4 µm thick poly-silicon cantilever with lengths of up two 500 µm that were released on 1 µm of thermal SiO_2 without sticking.

3.2 Dicing free release of fragile chips

Dicing of unpackaged microstructures is a big inconvenience. Unfortunately, many MEMS can not be sealed on a wafer scale that would allow the dicing of released structures using a standard wafer dicing machine with diamond blade and water jet for cooling. Today, wafers with the released structures are covered with a thick layer of photoresist, which is cured prior to dicing. The resist then has to be cleaned off the chips after the dicing procedure using a solvent, which involves different problems. Since the structures were released before the dicing the treatment in a liquid again involves the problem of sticking. On the other hand the dicing process creates small silicon particles which can redeposit on the wafer surface and travel into the small trenches of the MEMS while the photoresist is being cleaned off. These particles can provoke a shortcut of the electrostatic devices causing a failure of the device. Due to the small size of the non-fixed particles the failure can occur after complete assembly of the device or even during operation which causes high cost.

A clean method to release chips from the wafer without particle generating dicing is to use a double sided DRIE process and “dice” the chips with trenches that are etched during the same step as the MEMS structures (figure 5) [6]. To avoid a breaking of the wafer in the DRIE reactor the front- and the back-side trenches are

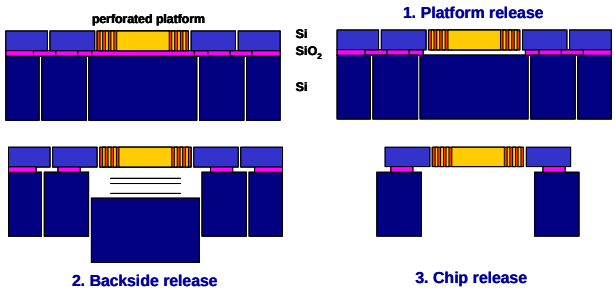

Figure 5: Double-sided deep reactive ion etching enables simultaneous release of the movable device, excess structures and chips on wafer level.

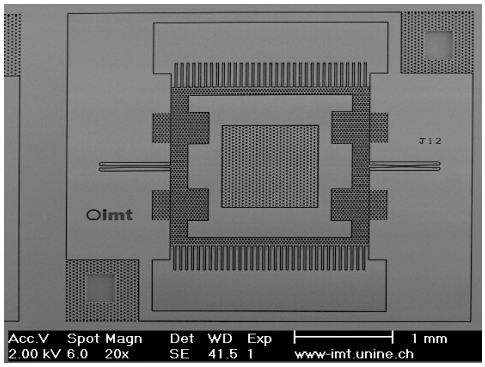

Figure 6: A large (> 1.5 x 1.5 mm^2) tiltable platform suspended by torsion beams was released and separated from the wafer during the same step.

etched with an overlapping area between the chip and a remaining frame. For release, the buried silicon dioxide of the overlapping area is etched away using HF vapour. This method enables a very clean release of extremely fragile structures without any mechanical impact on the chips. A large, tiltable platform was successfully fabricated and diced with this method (figure 6).

4 Conclusion

HF vapour phase etching offers a variety of new processing options for microsystem fabrication which enable the fabrication of new and very sophisticated devices. The technology is perfectly suitable for small and medium sized companies that cover niche markets where the cost per chip has a lower role than in so called “killer applications”. Some applications of HF vapour phase etching are given in this paper. For all in common is the strong increase of the fabrication yield, which is due to the quasi-dry etching of the sacrificial silicon dioxide. The presented dicing free MEMS release is often the only possibility to “dice” fragile chips without breaking the microstructures.

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